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(54) Method and apparatus for signal processing.

(57) A digital demodulator for a NICAM 728 system signal has sampling and digitizing means converting the signal into a succession of digital samples. The digital samples pass through an anti-aliasing digital comb filter to a selector (decimator) that selects one sample in three and feeds it to a second digital filter. Digital matched filters for the in-phase (I) and quadrature (Q) components of the signal effect the demodulation. Carrier and symbols I tracking is carried out digitally. A pulse-width modulated automatic gain control signal is produced for controlling the amplitude of the signal applied to the sampling and digitizing means.

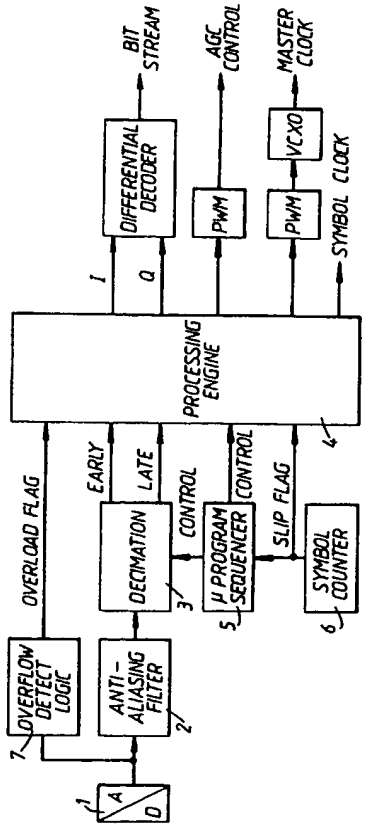

Fig.1.

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The present invention relates to signal processing and in particular to the digital processing of signals in a selected band of frequencies.

It is proposed to transmit high fidelity stereo sound signals in digital form in a television broadcast signal using a system known as NICAM 728 for which a specification has been published. In that system, the two sound signals forming the stereo pair are sampled, digitized, formed into digital frames and modulated using differential quadrature phase shift key (DQPSK) on to a carrier. The modulation is 4-state phase modulation in which each change of state conveys two data bits.

There are three versions of the system known as I, B and G respectively which differ from one another in the offset of the carrier for the NICAM signal from the broadcast carrier and the spectrum shaping. In the I system, the frequency offset is 6.552 MHz with a hundred per cent cosine roll-off split equally between the transmitter and the receiver. In the B and G systems, the frequency offset is 5.85 MHz with forty per cent cosine roll-off filtering. The B and G systems differ from one another in the separation between channels. In the B system, the channel separation is 7 MHz and in the G system it is 8 MHz.

As the NICAM 728 signal is additional to the television signal with its colour sub-carrier and FM sound, a television receiver for receiving the NICAM 728 signals requires additional circuitry for selecting and demodulating that signal. It would of course be possible to construct the demodulator using conventional techniques, but that would be relatively expensive. It is therefore an object of the present invention to enable the production of a selector and decoder for NICAM signals which is relatively less expensive and can possibly be constructed in the form of one or more integrated circuits with a minimum of additional components.

According to one aspect of the present invention there is provided signal processing apparatus including

an input circuit for receiving an input signal to be processed,

sampling and digitising means for repeatedly sampling the input signal and producing digital signals representing the samples,

first digital filtering means receiving the digital signals and producing output digital signals,

selecting means for regularly selecting the output digital signals representing one sample from each group of the output digital signals representing a plurality of successive samples,

second digital filtering means receiving the selected output digital signals, and

digital signal processing means responsive to the output signals from the second digital filtering means,

the characteristics of the first and second filtering means in conjunction with the operation of the selecting means producing an overall filter characteristic passing a desired band of frequencies with a predetermined spectrum shaping.

According to a second aspect of the present invention there is provided a method of processing an input signal including

repeatedly sampling the input signal and producing digital signals representing the samples,

subjecting the digital signal to a first digital filtering,

regularly selecting from the filtered digital signals those representing one sample from each group of such signals representing a plurality of successive samples,

subjecting the selected digital signals to a second digital filtering, and

applying the digital signals after the second digital filtering to digital signal processing means,

the characteristics of the first and second digital filtering in conjunction with the selection producing an overall filter characteristic passing a desired band of frequencies with a predetermined spectrum shaping.

The first digital filtering means may have a peak in the desired frequency band and one or more troughs in respective frequency bands which overlie the desired frequency band as a result of the operation of the selecting means. A suitable form for the first digital filtering means is a plurality of comb filters in cascade. The selecting means may be arranged to select one sample from each group of three samples.

The input signal may include representation of symbols at a second repetition rate which are derived from samples taken from an original signal at a first repetition rate, the sampling rate of the sampling and digitizing means may be a multiple of the first repetition rate and the operation of the selecting means may be modified periodically so that the mean repetition rate of the selected digital signal is a multiple of the second repetition rate. In the example of the invention to be described, the input signal is sampled at 16.384 MHz which is 512 x 32 kHz, the sampling rate used to produce the NICAM 728 signal. The symbol rate of the NICAM 728 signal is 364 kHz with the result that the number of samples per symbol is $45\frac{1}{91}$. In order that all parts of the system may be synchronised, the selecting means is adjusted to discard one sample after every 45 symbols.

Automatic gain control may be applied to an amplifier feeding the input signal to the sampling and digitizing means so as to reduce the dynamic range that the digitizing means has to handle. The automatic gain control signal may be derived by periodically processing samples from the signals from the second digital filtering means and producing a pulse width modulated output signal from the processed signals which can be smoothed

to produce the automatic gain control signal. The digitizing means may produce an overload signal when the input signal reaches a maximum value that can be digitized and that overload signal may be used to modify the automatic gain control signal.

The input signal may be a quadrature phase modulated signal, for example a NICAM 728 signal and the digital signal processing means may operate as a demodulator for such a signal and include two matched filters for the quadrature components of the signal and a rotator means responsive to the outputs of the matched filters to bring the signal to a reference phase. The signal processing means may subdivide the signals into groups representing symbols and may be arranged to adjust the position of that subdivision in response to the energy content of the groups.

The apparatus may comprise a suitably programmed microprocessor. The microprocessor may include two separate but linked processing units for respectively processing the two quadrature components.

An example of apparatus for demodulating a NICAM 728 system signal will now be described with reference to the accompanying drawings, of which:-

FIGURE 1 is a diagram of the architecture of the apparatus;
FIGURE 2 illustrates the operation of the first digital filtering means, the anti-alias filter;
FIGURE 3 shows the selecting means;
FIGURE 4 shows the structure of the processing engine of Figure 5;
FIGURE 5 symbols shows the I channel processing arm of Figure 4 and Figure 6 shows the Q processing arm of Figure 4;
FIGURE 7 shows the carrier tracking loop;
FIGUREs 8 and 9 show the alternative forms of loop filter for the carrier tracking loop;
FIGURE 10 shows the automatic gain control loop;
FIGURE 11 shows the automatic gain control overload protection circuit;
FIGURE 12 shows the pulse width modulators of Figure 1;
FIGURE 13 is the constellation diagram of a NICAM 728 DQPSK modulated signal;
FIGURE 14 shows the energy changes from one symbol to the next;
FIGURE 15 shows the control loop for tracking the symbols;
FIGURE 16 illustrates the entire NICAM data demodulation algorithm; and
FIGURE 17 shows the architecture of a feedforward equalizer.

The invention will be described with reference to a demodulator for NICAM 728 system signals implemented in the form of a digital signal processor, possibly as a single integrated circuit chip, controlled by a special program producing algorithms for effecting the required processing of the signals. In the following description the algorithms are illustrated as circuit configurations and can be implemented in that way.

Figure 1 illustrates the main fonctional blocks which performs the data demodulation function. The architecture internal to each of these blocks is discussed in the following sections.

The analogue to digital converter I samples the input signal at 16.384 MHz and produces a 6-bit parallel output which is applied to the anti-alias filter 2.

Figure 2 gives the architecture of the anti-alias filter. This filter rejects the alias bands A_1 and A_2 which are aliased into the NICAM band by the subsequent decimation process. The filter is a cascade of three comb filters.

The final comb filter stage is 'programmable' in that it implements an A2 comb filter in the case of System I or implements an S2 filter in the case of System B/G. The three additions result in three bits being added to the number resolution.

The top 8 bits of the 9 bit result of the final addition/substraction are propagated forward to the decimator.

The decimator 3 performs two functions :

1. Reduction in sample rate from 16.384 MHz (nominal) to 5.46133 MHz (nominal), ie, a decimate by 3.
2. Implementation of slip function to maintain symbol tracking lock.

Figure 3 shows the architecture of the decimator 3.

In the operation of the decimator two clocking signals 'early in' and 'late in' are derived from the microprogram sequencer 5, and perform the sub-sampling of the anti-alias filter output to derive the early and late sample streams which feed the matched filters.

Under the normal operating conditions (non-slip event) the 'early in' and 'late in' signals are identical, thus providing the same phase of information to the early/late filters which make up the matched filters in the processing engine 4. Every 91 symbols a sample from the comb filter output must be discarded to maintain symbol lock. This event is termed the 'slip event'. To maintain coherency across the matched filtering window of two symbols the slip event effects two symbols. In the first symbol a sample is deleted from the stream used to derive the early data stream. In the second symbol a sample is deleted from the stream used to derive the late

data stream.

Notice that after the first symbol of the slip event the phase of the early/late data streams are returned to their normal operating conditions. Notice also that this is achieved by inserting an additional instruction (inst 45) into the microprogram sequence.

For compability with the Philips D/A convertors the final output sample stream is required to be synchronized to a 16.384 MHz master clock, this master clock being an exact multiple of the output sample rate of 32 kHz. The symbol rate (364 kHz) is, however, not an integer dividend of 16.384 MHz. Hence the use of an A/D sampling frequency of 16.384 MHz results in a non-integer number of samples per symbol ($45\frac{1}{91}$) . Since the matched filters assume an integer number of samples/symbol, then the incoming symbol stream is contunially advancing (by one sample every 91 symbols with respect to the operation of the matched filters. However, by deleting one sample every 91 symbols the operation of the matched filters may be synchronized to the symbol rate. Thus all parts of the system may be synchronized.

The symbol conter 6 is a modulo 91 counter which is used to count out the inter-slip duration of 91 symbols. Clearly this counter is clocked at the symbol rate.

The overflow detection logic 7 is used as a fail safe mechanism where the AGC loop drives the front end into saturation. One detection of a full scale value on the A/D output the overflow flag is set for the duration of the subsequent symbol.

The processing engine 4 perfoms the vast majority of the data demodulating function including:

1. Matched filtering
2. AGC
3. Carrier tracking
4. Symbol tracking

The processing engine is best considered as consisting of two near identical processing arms with additional support circuitry. Figure 4 gives a block diagram description of the processing engine. The processing arms operate in parallel running separate programs to perform the demodulation. They can communicate via dedicated communications channels at specific times. Each arm is controlled separately by the microprogram ROM 8.

Figures 5 and 6 give a detailed description of the architecture internal to the I and Q processing arms 9 and 10 respectively. Comparison of Figures 5 and 6 will show that the two arms differ slightly in operand selection circuitry. Each arm of the architecture can execute an intruction of the form :

Register = (holding register) = Z[+ / - /plus]result_shift(X * Y)

or

Register = (holding register) = Z[+ / - /plus] W

where

Register	= any 16 bit register in this channel's register file.
Z	= any non-shifted 17 bit (see note 1 below) register in either channel's register file or local special 16 bit constant registers.
W	= any 16 bit register in either channel's register file. Register value may be shifted by Shift B (Q channel only), Shift C (I channel only) or unshifted (see below for definition of shift B and shift C operations).
X	= 8 bit 'late' input from the decimator. 8 bit ROM value, The 8 bit 2's complement representation of the sign (ie. +/-1) of any value held in the local register file. The 8 bit 2's complement representation of the sign (ie. +/-1) of the Y parameter at the multiplier input.
Y	= 8 bit 'early' input from the decimator, 8 bit ROM value, The bottom eight bits of any value held in either channel's register file, The 8 bit result of shift A on the contents of any register in either channel's register file (see below for definition of shift A operation)

[+ / - / plus] means either '+' or ' -' or 'plus'

+	= 16 bit addition (Z + W) with saturation.
-	= 16 bit subtraction (Z - W) with saturation.
plus	= 16 bit addition (Z + W) without saturation (ie. modulo

FFFF hex) - NON FILTERING INSTRUCTIONS

17 bit addition (Z + W) without saturation (ie. modulo 1FFFF hex) - EARLY/LATE FILTERING INSTRUCTIONS

result_shift (X * Y) is either :

No_shift (X * Y) = directly the 16-bit multiplier output.

Lshift (X * Y) = the 16 bit-multiplier output left shifted two places (the sign bit being preserved and a '0' used as the two LSbs) saturation logic is required:

```
if ( (X * Y) >= 8192) )
    L shift (X * Y) = 32767;

else
  {
   if ( (X * Y) <= -8192) )
        Lshift(X * Y) = -32768;
else
        Lshift(X * Y) = (X * Y) << 2
  }
```

Definition of multiplier input operand (Y) shifting operations

Shift A = output = input >>8 (with sign extension)

Definition of adder/subtractor input operand (W) shifting operations

Shift B = output = input >>12 (with sign extension)

Shift C = output = input >>2 (with sign extension)

note 1: Only two registers within the register file are 17 bits wide (namely acc_A and acc_B) the remainder are 16 bits wide. In the case of a Z operand fetch from any of the 16 bit registers the 17th bit is identical to the 16th bit (See Figure 4.10. Acc_A and Acc_B are used exclusively to perform the early/late filtering.

Non saturating 17-bit arithmetic is used for the first 14 of the 15 multiply-accumulate instructions which make up each of the early/late filtering operations. The last (15th) instruction takes a 17 bit Z operand but saturates the result to 16 bits. Roll around of the accumulated result within the first 14 instructions is not possible under any operating conditions since the A/D cannot supply sufficiently large values, even when saturating.

Restriction include (See architecture):

1. The special constant registers are rad only registers.
2. The holding registers are write only registers.

The instructions format illustrates that any result operand may be optionally copied into a particular holding register whilst performing the result write back to the local register file. This avoids he need for additional instructions being required to copy data from the register file to the special registers. The holding registers are HR0, HR1, HR2, HR3 and HR4. The 16 bit constant registers are angle_increment and AGC_nominal.

Each arm executes a similar purely sequential program with no branches (other than the branch back to instruction zero at the end of the program). Both programs consist of 46 instructions. These 46 instructions are best considered as 15 consecutive 3 line sub-programs followed by a single optional NOP instruction. Each sub-process is distinct. Normally the micro-instruction address cycles back to zero after instruction 44. However, if the slip request flag is high at the end of instruction 44 the conditional NOP instruction is executed before cycling back round to instruction 0. Hence the conditional NOP is a conditional instruction 45.

The second and third instruction in each sub-program manipulate the late and early input samples respectively and perform the matched filtering of the input signal. These instructions are common to both processing 'arms', although the filter coefficients fetched are different for each arm and depend on the system modulation (ie. I or B/G). The first instruction in each sub-program is also channel dependent (ie. I or Q), and is available to perform the remainder of all the processing.

The processing arms are required to communicate in order to perform the various tracking functions. Inter-arm communications is performed via the cross coupling of the 'B' busses on the register file outputs. To avoid bus contention the other channel is prevented from using this bus during the transfer. There are two modes of

operation of the processing arms, namely :

Local mode : where each processing arm can access a register in its local register file via its ' B' bus.

Cross channel mode : where each processing arm can access a register in the other channel's register file via the ' B' bus of the other arm.

Thus contention is avoided by restricting both arms to be operating in the same mode for a given instruction.

The processing arms communicate with the rest of the architecture via the five holding registers HR0, HR1, HR2, HR3 and HR4. The holding registers are write only registers. HR0 and HR2 appear in arm I's address space whereas HR1, HR3 and HR4 appear in arm Q's address space.

Two ROMs are used in the processing engine architecture, namely:

1) I-Rom, Q-ROM : 128 words x 16 bits

Note : the upper eight bits holds I values and the lower eight bits hold Q values.

2) COS-ROM : 128 words x 8 bits

The two ROM's may be combined in a single ROM.

The I_ROM ROM is used exclusively by the I processing arm. Similarly the Q_ROM ROM is used exclusively by the Q processing arm. The COS_ROM provide the sin/cos lookup table function and is accessed by both processing arms. The COS_ROM is accessed twice per symbol, once to fetch a cosine value and once to fetch a sine value. The value fetched in both cases is fed to both processing arms. A part form these two COS_ROM accesses each processing arm uses only its associated ROM to fetch constants.

The bottom 6 bits of ROM addressing for the I_ROM and Q_ROM is provided by the current microprogram address, thus reducing the micro instruction decode ROM width. The MSb of the ROM address is provided by the System I/System BG flag.

Since the micro program address generator may not generate a valid address bigger than 45 then the ROM locations 46 to 63 inclusive and 110 to 127 inclusive in ROM I_ROM Q_ROM are never accessed.

The ROM addressing for the COS_ROM is provided by the contents of holding register HR4 which contains the result of the carrier tracking algorithm (angle). The 8 bit contents of this register is pre-processed to yield a 7 bit result which is then used to address the COS_ROM. The sin/cos look up may be defined as :

case 1: COSINE TABLE ACCESS

COS(angle) = COS_ROM (address)

where address is given by

case a: Msb of angle is zero
address = seven LS bits of angle

case b: Msb of angle is one
address = seven LS bits of angle INVERTED

case 2: SINE TABLE ACCESS

SIN(angle) = COS(angle ÷ 64):

Note: The I_ROM and Q_ROM could equivalently be implemented either by a single 128 by 16 wide ROM or two 128 x 8 bit ROMs.

It should be noted that the content of the COS_ROM at address ' N' is defined by

$$[127 * COS(N\pi/128 + \pi/256)]$$

where [ ] denotes rounding to the nearest integer.

The circular buffer consists of two registers in each arm, referred to as circular_buffer{n-1} and circular_buffer{n-2}. When these registers are accessed the lsb of the register address is provided not directly by the microcode, but is XOR'd with a flip-flop output which toggles on each symbol. Hence the actual register accessed as circular-buffer{n-1} toggles from symbol to symbol circular_buffer{n-2} also toggles between RF3, RF2 re-

spectively.

The optimum filter for demodulation of the NICAM signal is the matched filter. The matched filter is defined by equation 1.15.

$$H(f) = \frac{KD(f)}{G_I(f)} \quad (1.15)$$

where

$H(f)$ = Matched filter response
$D(f)$ = Wanted signal spectrum
$G_I(f)$ = Interference signal power spectral density function
K is an arbitrary constant which may be ignored.

The digital equivalent of equation 1.15 is given by equation 1.16.

$$H(z) = \frac{D(z)}{G_I(z)} \quad (1.16)$$

Transforming back to the time domain and utilising the Wiener-Khintchine theorem, equation 1.15 becomes

$$\Phi_{II}(t) * H(t) = D(t) \quad (1.17)$$

where

* denotes convolution.

$\Phi_{II}(t)$ = autocorrelation function of the interference signal. (1.18)

In the case where the interference signal may be assumed to be uncorrelated from sample to sample (i.e. it has a " white" spectrum) then

$$\Phi_{II}(t) = \delta(t) \quad (1.19)$$

and equation 1.17 reduces to the well known result

$$H(t) = D(t) \quad (1.20)$$

i.e. that the matched filter has the same response as the wanted signal.

In the case of the NICAM signal, the interfering signals are not uncorrelated, being derived from a composite TV signal. Consequently, the optimum matched filter needs to be designed by consideration of a realistic interfering FM sound and video signal.

In the case of system I, each of the arm filters in I and Q arms are implemented as a cascade of the comb filters with an FIR filter of duration 2 symbols running at one third of the input sample rate. The coefficients of the FIR filters for system I are derived using a procedure which optimizes the overall response of the cascade of the comb filters with the FIR filter. The coefficients used are:

HI(0)	=	5/256	HQ(0)	=	2/256
HI(1)	=	-2/256	HQ(1)	=	5/256
HI(2)	=	-6/256	HQ(2)	=	2/256
HI(3)	=	0/256	HQ(3)	=	-3/256
HI(4)	=	1/256	HQ(4)	=	1/256
HI(5)	=	-9/256	HQ(5)	=	0/256
HI(6)	=	-2/256	HQ(6)	=	-18/256
HI(7)	=	32/256	HQ(7)	=	-11/256
HI(8)	=	28/256	HQ(6)	=	40/256
HI(9)	=	-46/256	HQ(9)	=	52/256
HI(10)	=	-80/256	HQ(10)	=	-38/256
HI(11)	=	20/256	HQ(11)	=	-106/256
HI(12)	=	123/256	HQ(12	=	-12/256
HI(13)	=	49/256	HQ(13)	=	127/256
HI(14)	=	-113/256	HQ(14)	=	86/256
HI(15)	=	-113/256	HQ(15)	=	-87/256
HI(16)	=	49/256	HQ(16)	=	-127/256
HI(17)	=	123/256	HQ(17)	=	12/256
HI(18)	=	20/256	HQ(18)	=	106/256
HI(19)	=	-80/256	HQ(19)	=	38/256
HI(20)	=	-46/256	HQ(20)	=	-52/256
HI(21)	=	28/256	HQ(21)	=	-40/256
HI(22)	=	32/256	HQ(22)	=	11/256
HI(23)	=	-3/256	HQ(23)	=	18/256
HI(24)	=	-9/256	HQ(24)	=	0/256
HI(25)	=	1/256	HQ(25)	=	-1/256
HI(26)	=	0/256	HQ(26)	=	3/256
HI(27)	=	-6/256	HQ(27)	=	-1/256
HI(28)	=	-2/256	HQ(28)	=	-4/256
HI(29)	=	5/256	HQ(29)	=	-2/256

In the case of systems B and G, the performance of the matched filter is inadequate if the length of the matched filter is limited to 2 symbols duration. In order to overcome that difficulty a feedfoard equalizer is used to extend the effective time window of the matched filter as shown in Figure 16, allowing both ISI to be reduced, and allowing greater frequency resolution. Figure 17 illustrates how the feedforward equalizer works. The FFE is essentially an FIR filter whose inputs are the outputs from the matched filter, sampled at the centre of each symbol. The FFE thus operates at the symbol rate and for an 'N' tap filter has a time window of N symbols. The central symbols value S(n-N/2) is the symbol currently being processed. This symbol value has a weighted sum of contributions from its adjacent removed. The intention is that the filter coefficients are indicative of the ISI contributions from adjacent symbols. For symmetrical symbol waveforms such as NICAM the ISI contributions from symbols symmetrically placed either side of the central symbol will be identical. Hence:

$$K_L = K_{L-N-1} \qquad O \leqq L \leqq (N/2 - 1)$$

In the case of systems B and G, each of the arm filters in the I and Q arms are implemented as a cascade

of the comb filters, an FIR filter of duration 2 symbols running at one third of the input sample rate and a feedforward equalizer of length 3 symbols. The coefficients of the FIR filter and the feedforward equalizer are derived using a procedure which optimizes the overall response of the cascade of the comb filters, the FIR filters and the feedforward equalizer. The coefficients used are:-

FFEI(0)	= -52/256	FFEQ(0)	= -52/256
FFEI(1)	= 1	FFEQ(1)	= 1
FFEI(2)	= -52/256	FFEQ(2)	= -52/256

HI(0)	= 22/256	HQ(0)	= 3/256
HI(1)	= 18/256	HQ(1)	= 9/256
HI(2)	= 8/256	HQ(2)	= 18/256
HI(3)	= -3/256	HQ(3)	= 29/256
HI(4)	= -16/256	HQ(4)	= 37/256
HI(5)	= -30/256	HQ(5)	= 38/256

HI(6)	=	-44/256	HQ(6)	=	27/256
HI(7)	=	-56/256	HQ(7)	=	5/256
HI(8)	=	-62/256	HQ(8)	=	-25/256
HI(9)	=	-57/256	HQ(9)	=	-55/256
HI(10)	=	-36/256	HQ(10)	=	-77/256
HI(11)	=	-2/256	HQ(11)	=	-86/256
HI(12)	=	39/256	HQ(12)	=	-79/256
HI(13)	=	75/256	HQ(13)	=	-55/256
HI(14)	=	97/256	HQ(14)	=	-20/256
HI(15)	=	97/256	HQ(15)	=	20/256
HI(16)	=	75/256	HQ(16)	=	55/256
HI(17)	=	39/256	HQ(16)	=	79/256
HI(18)	=	-3/256	HQ(18)	=	86/256
HI(19)	=	-36/256	HQ(19)	=	77/256
HI(20)	=	-56/256	HQ(20)	=	54/256
HI(21)	=	-62/256	HQ(21)	=	24/256
HI(22)	=	-56/256	HQ(22)	=	-5/256
HI(23)	=	-44/256	HQ(23)	=	-27/256
HI(24)	=	-30/256	HQ(24)	=	-38/256
HI(25)	=	-16/256	HQ(25)	=	-37/256
HI(26)	=	-3/256	HQ(26)	=	-29/256
HI(27)	=	9/256	HQ(27)	=	-18/256
HI(28)	=	18/256	HQ(28)	=	-9/256
HI(29)	=	22/256	HQ(29)	=	-3/256

The matched filters only operate successfully when the phase of the carrier for each symbol is the same as the reference phase used in the matched filters. The received carrier may, however, have any arbitrary phase, which will vary with time due to transmitted carrier frequency drift and the local sampling rate variations. The carrier lock loop is required to calculate the phase difference angle, and rotate the output of the matched filters accordingly.

Consider the operation of the matched filter which is matched to the inphase component of the NICAM signal. The NICAM signal may be represented by

$$z(t) = I_K D(t)\cos(wct - \phi) - Q_K D(t)\sin(wct + \phi) \quad (1.36)$$

The impulse response of this matched filter $P_I(t)$ is thus given by

$$P_I(t) = AD(t)\cos wct \quad (1.37)$$

where A is an arbitrary gain constant.

If the matched filter is considered as an ideal correlation receiver then $VOI(KT_S)$, the in-phase component output by a matched filter, is given by:-

$$VOI(KT_S) = \int_{-\infty}^{\infty} P_I(t)z(t)dt \quad (1.38)$$

Since

$$\cos(wct + \phi) = \cos wct \cos \phi - \sin wct \sin \phi \quad (1.39)$$
$$\sin(wct + \phi) = \sin wct \cos \phi + \cos wct \sin \phi \quad (1.40)$$

then

$$VOI(KT_S) = A\cos\phi \int_{-\infty}^{\infty} I_K D^2(t)\cos^2 wct\,dt$$

$$+ A\sin\phi \int_{-\infty}^{\infty} Q_K D^2(t)\cos^2 wct\,dt$$

$$+ A\cos\phi \int_{-\infty}^{\infty} I_K D^2(t)\sin wct\cos wct\,dt$$

$$- A\sin\phi \int_{-\infty}^{\infty} Q_K D^2(t)\sin wct\cos wct\,dt \qquad (1.41)$$

The third and fourth integrals are integrals of an odd function over symmetric limits and thus integrate to zero.

Hence

$$VOI(KT_S) = I_K A\cos\phi \int_{-\infty}^{\infty} [D(t)\cos wct]^2\,dt$$

$$+ Q_K A\sin\phi \int_{-\infty}^{\infty} [D(t)\cos wct]^2\,dt \qquad (1.42)$$

now $D(t)\cos wct$ corresponds to the baseband pulse shape modulated onto a cosine carrier. The power spectral density function $G_z(f)$ is given by

$$\int_{-\infty}^{\infty} G_z(f)df = \int_{-\infty}^{\infty} (D(t)\cos wct)^2\,dt \qquad (1.43)$$

Hence

$$VOI(KT_s) = I_K A\cos\phi \int_{-\infty}^{\infty} G_z(f)df + Q_K A\sin\phi \int_{-\infty}^{\infty} G_z(f)df \qquad (1.44)$$

If E is the energy within the symbol due to the inphase component then

$$\int_{-\infty}^{\infty} G_z(f)df = E \qquad (1.45)$$

Hence

$$VOI(KT_S) = [I_K \cos\phi + Q_K \sin\phi] \cdot AE \qquad (1.46)$$

Similarly for the quadrature component

$$VOQ(KT_S) = [-I_K \sin\phi + Q_K \cos\phi] AE \qquad (1.47)$$

The above results may be obtained directly by resolving the inphase and quadrature components onto the reference vectors with the gain A equal to unity.

$$I_{o/p} = IREF.(I_K + Q_K) \qquad (1.48)$$

$$= E[I_K \cos \phi + Q_K \sin \phi] \quad (1.49)$$

$$Q_{o/p} = QREF.\ (I_K + Q_K) \quad (1.50)$$

$$= E[-I_K \sin \phi + Q_K \cos \phi] \quad (1.51)$$

Hence we may correct fr phase error by rotating the output of the filters thus

$$I_K E = \cos \phi . VOI\ (KT_S) - \sin \phi VOQ\ (KT_S) \quad (1.52)$$

$$Q_K E = \sin \phi . VOI(KT_S) + \cos \phi VOQ\ (KT_S) \quad (1.53)$$

ie the correct I and Q outputs I' and Q' are given by

$$\begin{bmatrix} I' \\ Q' \end{bmatrix} = \begin{bmatrix} \cos\phi & -\sin\phi \\ \sin\phi & \cos\phi \end{bmatrix} \begin{bmatrix} I \\ Q \end{bmatrix} \quad (1.54)$$

The angle ø may be calculated from $VOI(KT_S)$ and $VOQ(KT_S)$ by base-band remodulation. That is implemented by the right-band side of Figure 7.

Assuming that the limiters produce the original baseband signal I_K and Q_K then y is given by

$$y = E[Q_K I_K \cos \phi + Q_K^2 \sin \phi] - E[I_K Q_K \cos \phi - I_K^2 \sin \phi] \quad (1.55)$$

$$= + 2E \sin \phi \ (\text{since } I_K^2 = Q_K^2 = E) \quad (1.56)$$

Given sin ø may use a look up table for cos ø and hence generate the rotation matrix, or alternatively, since the loop will be nominally operting in lock, ø may be assumed to be small so that $\phi \approx \sin \phi$.

Returning to the assumption that I_K and Q_K are obtained at the output of the limiters, this assumption is valid if

$$\cos \phi = \sin \phi > 0 \quad (1.57)$$

ie if

$$\phi < \frac{\pi}{4} \quad (1.58)$$

Since the reference carrier arbitrarily be any be any one of four vectors spaced $\frac{\pi}{2}$ apart then the incoming NICAM carrier cannot be more than $\frac{\pi}{4}$ from a possible reference carrier position. Therefore the assumption is valid in the absence of interference.

Figure 7 illustrates the carrier tracking loop. The loop filter 20 provides a feedback path between the base-band remodulator and the rotator.

The required ideal characteristics of the carrier loop filter are:

1. Zero steady state error ($E(z)$) as a result of a step change in ø(z). A step change in ø(z) arises if the incoming NICAM carrier has a fixed non-zero phase offset with respect of the local carrier phase.
2. Zero steady state error ($E(z)$) as a result of a ramp change in ø(z). A ramp change in ø(z) is obtained if the incoming NICAM carrier has a fixed frequency offset relative to the local carier frequency. This situation will occur due to transmitter inter-carrier drift and variations in sampling clock frequency.
3. Zero phase jitter on the estimate of carrier phase ø(z). The output of the baseband remodulator will be corrupted by ISI, noise and residual TV signal interference. Ideally the carrier loop filter should remove this jitter component by providing sufficient attenuation of the frequency components which make up this jitter signal.

Figure 8 shows the architecture of a suitable loop filter.

As discussed previously, the output of the baseband remodulator is corrupted by residual interference. This gives rise to ' Jitter' on the carrier tracking error estimate. This Jitter is filtered by the loop filter and leads to corruption of the rotation angle used by the rotator, thereby degrading system performance. In order to reduce the residual jitter at the output of the loop filter the loop filter gain and bandwith are required to be reduced. This causes the response time of the closed loop transfer function to be correspondingly increased. Hence there is a trade-off between setting time and jitter performance.

The baseband remodulator performs the estimation of carrier tracking error on a symbol to symbol basis. This estimate is only valid if the carrier tracking error remains constant for the duration of each symbol. Hence, in the case of a frequency offset between the received carrier and local carrier reference, the carrier tracking error estimate provided by the baseband remodulator is in error. This error is related to the frequency offset (fdiff) between the local and received carriers and the symbol rate, ie.

$$\text{error } \alpha \frac{2\pi \text{fdiff}}{\text{symbol rate}}$$

In the case of fdiff = 1 kHz for System I, the error was found to be approximately 0.006 radians. Hence

the constant of proportionality is ≈ 0.35.

The carrier loop filter shown in Figure 8 is a design based on the zero steady state error requirements. It can be shown that even with this ' ideal' filter structure the steady state error will in fact be non-zero. This result leads to the conclusion that a simplified filter structure (which does not necessarily meet the zero steady state error requirements) could be used with negligible loss in performance, provided that the theoretical steady state error is small compared to expected degradation due to the baseband remodulator corruption of carrier tracking error (or small compared to the residual jitter). The architecture of a simpler loop filter designed on that basis is shown in Figure 9.

The simplified loop filter is a cascade of a single integrator and a lowpass filter (See Figure 9 and requires one less accumulator than the ' ideal' filter given previously. The presence of the single integrator guarantees zero steady state error in response to step change in phase difference. The steady state error in response to a ramp change in phase difference is

$$\left(\frac{P-1}{KG}\right)\cdot\frac{2\pi fdiff}{fsym}$$

Hence for equivalent performance with the loop filter shown in Figure 8 then

$$\left|\frac{P-1}{KG}\right| << 0.3$$

If the DC gain of the lowpass section is normalised, ie.

$$K = K_v(1 - P)$$

then the requirement becomes

$$\frac{1}{K_vG} << 0.35$$

$$\Rightarrow K_v >> 2.85 \text{ for } G \approx 1$$

Claims

1. Signal processing apparatus including
an input circuit for receiving an input signal to be processed,
sampling and digitising means for repeatedly sampling the input signal and producing digital signals representing the samples,
first digital filtering means receiving the digital signals and producing output digital signals,
selecting means for regularly selecting the output digital signals representing one sample from each group of the output digital signals representing a plurality off successive samples,
second digital filtering means receiving the selected output digital signals, and
digital signal processing means responsive to the output signals from the second digital filtering means,
the characteristics of the first and second filtering means in conjunction with the operation of the selecting means producing an overall filter characteristic passing a desired band of freqencies with a predetermined spectrum shaping.

2. Apparatus according to claim 1, wherein the characteristic of the first digital filtering means has a peak in the desired freqency band and one or more troughs in respective frequency bands which overlie the desired freqency band as a result off the operation of the selecting means.

3. Apparatus according to claim 2, wherein the first digital filtering means comprises a plurality of comb filters in cascade.

4. Apparatus according to claim 2 or claim 3, wherein the selecting means selects the output digital signals representing one sample from each group of the output digital signals representing three samples.

5. Apparatus according to any one of the preceding claims, wherein the input signal includes representations

of symbols produced at a second repetition rate and derived from samples taken from an original signal at a first repetition rate, the sampling rate off the sampling and digitising means is a multiple of the first repetition rate, and the operation of the selecting means is periodically modified so that the mean repetition rate of the selected output digital signals from the selecting means is a multiple of the second repetition rate.

6. Apparatus according to any one of the preceding claims, wherein the digital signal processing means includes means for periodically processing samples from the signals it receives from the second digital filtering means and means for producing a pulse-width modulated output signal from the processed samples, the pulse-width modulated output signal being usable after smoothing as an automatic gain control signal for limiting the dynamic range of the input signal applied to the apparatus.

7. Apparatus according to claim 6, wherein the sampling and digitising means is arranged to produce an overload signal when the input signal reaches a maximum value that can be digitised, the overload signal being usable to modify the automatic gain control signal.

8. Apparatus according to any one of the preceding claims, wherein the input signal is a quadrature phase modulated signal and the digital signal processing means operates as a demodulator and includes two matched filters for the quadrature components of the signal and rotator means responsive to the outputs off the matched filters for adjusting the values of the signal components so that the signal is in a reference phase.

9. Apparatus according to claim 8, wherein the signal processing means includes means for subdividing the signals received from the second digital filtering means into groups representing symbols and for adjusting the position of the subdivision in response to the energy content of the groups so as to correct the subdivision of the signals into groups representing symbols.

10. Apparatus according to claim 9 in which the sampling and digitizing means includes oscillator means for determining the instants of sampling the input signal, the oscillator means also operating the selecting means, wherein the frequency of oscillator means is adjustable in response to the energy content of the groups of signals representing symbols.

11. Apparatus according to any one of the preceding claims, wherein all the digital signal handling means and the interconnections between them are provided by a suitably programmed microprocessor.

12. Apparatus according to claim 8, 9 or 10, wherein all the digital signal handling means are provided by suitable programmed microprocessor means having two separate processing units for respectively processing the two quadrature components with similar and co-operating programs, each of the processing units having access to storage registers of the other of the processing units.

13. Apparatus according to claim 8, 9 or 12, wherein the input signal is a differential qadrature phase shift keying modulated signal.

14. Apparatus according to claim 12, wherein the input signal includes a NICAM 728 signal.

15. Apparatus according to claim 14 for demodulating an I system signal in which the coefficients of the I and Q channel matched filters are:

HI(0) =	5/256	HQ(0) =	2/256
HI(1) =	-2/256	HQ(1) =	5/256
HI(2) =	-6/256	HQ(2) =	2/256
HI(3) =	0/256	HQ(3) =	-3/256
HI(4) =	1/256	HQ(4) =	1/256
HI(5) =	-9/256	HQ(5) =	0/256
HI(6) =	-2/256	HQ(6) =	-18/256
HI(7) =	32/256	HQ(7) =	-11/256
HI(8) =	28/256	HQ(6) =	40/256
HI(9) =	-46/256	HQ(9) =	52/256
HI(10) =	-80/256	HQ(10) =	-38/256
HI(11) =	20/256	HQ(11) =	-106/256
HI(12) =	123/256	HQ(12 =	-12/256
HI(13) =	49/256	HQ(13) =	127/256
HI(14) =	-113/256	HQ(14) =	86/256
HI(15) =	-113/256	HQ(15) =	-87/256
HI(16) =	49/256	HQ(16) =	-127/256
HI(17) =	123/256	HQ(17) =	12/256
HI(18) =	20/256	HQ(18) =	106/256
HI(19) =	-80/256	HQ(19) =	38/256
HI(20) =	-46/256	HQ(20) =	-52/256
HI(21) =	28/256	HQ(21) =	-40/256
HI(22) =	32/256	HQ(22) =	11/256
HI(23) =	-3/256	HQ(23) =	18/256
HI(24) =	-9/256	HQ(24) =	0/256
HI(25) =	1/256	HQ(25) =	-1/256
HI(26) =	0/256	HQ(26) =	3/256
HI(27) =	-6/256	HQ(27) =	-1/256
HI(28) =	-2/256	HQ(28) =	-4/256
HI(29) =	5/256	HQ(29) =	-2/256

16. Apparatus according to claim 14 for demodulating a B or G system signal in which the coefficients of the I and Q channel matched filters are:

HI(0)	=	22/256	HQ(0)	=	3/256
HI(1)	=	18/256	HQ(1)	=	9/256
HI(2)	=	8/256	HQ(2)	=	18/256
HI(3)	=	-3/256	HQ(3)	=	29/256
HI(4)	=	-16/256	HQ(4)	=	37/256
HI(5)	=	-30/256	HQ(5)	=	38/256
HI(6)	=	-44/256	HQ(6)	=	27/256
HI(7)	=	-56/256	HQ(7)	=	5/256
HI(8)	=	-62/256	HQ(8)	=	-25/256
HI(9)	=	-57/256	HQ(9)	=	-55/256
HI(10)	=	-36/256	HQ(10)	=	-77/256
HI(11)	=	-2/256	HQ(11)	=	-86/256
HI(12)	=	39/256	HQ(12)	=	-79/256
HI(13)	=	75/256	HQ(13)	=	-55/256
HI(14)	=	97/256	HQ(14)	=	-20/256
HI(15)	=	97/256	HQ(15)	=	20/256
HI(16)	=	75/256	HQ(16)	=	55/256
HI(17)	=	39/256	HQ(16)	=	79/256
HI(18)	=	-3/256	HQ(18)	=	86/256
HI(19)	=	-36/256	HQ(19)	=	77/256
HI(20)	=	-56/256	HQ(20)	=	54/256
HI(21)	=	-62/256	HQ(21)	=	24/256
HI(22)	=	-56/256	HQ(22)	=	-5/256
HI(23)	=	-44/256	HQ(23)	=	-27/256
HI(24)	=	-30/256	HQ(24)	=	-38/256
HI(25)	=	-16/256	HQ(25)	=	-37/256
HI(26)	=	-3/256	HQ(26)	=	-29/256
HI(27)	=	9/256	HQ(27)	=	-18/256
HI(28)	=	18/256	HQ(28)	=	-9/256
HI(29)	=	22/256	HQ(29)	=	-3/256

and the outputs of the matched filters are applied to feedforward equalizers respectively for the I and Q channels having the coefficients:

FFEI(0) = -52/256 FFEQ(O) = -52/256
FFEI(1) = 1 FFEQ(1) = 1
FFEI(2) = -52/256 FFEQ(2) = -52/256

17. Signal processing apparatus substantially as described herein and as illustrated by the accompanying drawings.

18. A method of processing an input signal including
repeatedly sampling the input signal and producing digital signals representing the samples,
subjecting the digital signal to a first digital filtering,

regularly selecting from the filtered digital signals those representing one sample from each group off such signals representing a plurality off successive samples,

subjecting the selected digital signals to a second digital filtering, and

applying the digital signals after the second digital filtering to digital signal processing means,

the characteristics of the first and second digital filtering in conjunction with the selection producing an overall filter characteristic passing a desired and of frequencies with a predetermined spectrum shaping.

19. A method according to claim 18, wherein thecharacteristic of the first digital filtering has a peak in the desired frequency band and one or more troughs in respective freqency bands which overlie the desired freqency band as a result of the selection operation.

20. A method according to claim 19, wherein the first digital filtering has the characteristic of a plurality of comb filters in cascade.

21. A method according to claim 19 or claim 20, wherein the selecting is such that the digital signals representing one sample are selected from each group of digital signals representing three samples.

22. A method according to any one of claims 18 to 20, wherein the input signal includes representations of symbols produced at a second repetition rate and derived from samples taken from an original signal at a first repetition rate, the sampling rate applied to the input signal being a multiple of the first repetition rate and the selection being periodically modified so that the mean repetition rate of the selected digital output signals is a multiple off the second repetition rate.

23. A method according to any one of claims 18 to 22, wherein the digital signal processing means operates to process periodically samples from the signals it receives and produces a pulse-width modulated output signal from the processed samples, the pulse-width modulated output signal being usable after smoothing as an automatic gain control signal for limiting the dynamic range of the input signal.

24. A method according to claim 23, including producing an overload signal when the input signal reaches a maximum value that can be digitised, the overload signal being usable to modify the automatic gain control signal.

25. A method according to any one of claims 18 to 24, wherein the input signal is a quadrature phase modulator signal and the digital signal processing means operates as a demodulator applying matched filters to the quadrature components of the signal and being responsive to the values of those components to adjust them so that the signal is in a reference phase.

26. A method according to claim 25, wherein the signal processing means subdivides the signals it receives into groups representing symbols, adjusting the position of the subdivision in response to the energy content of the groups.

27. A method according to claim 26 wherein the frequency of an oscillation is adjusted in response to the energy content of the groups, the oscillator determining the instants of sampling the input signal and the position of the subdivision into groups.

28. A method according to claim 25, 26 or 27, wherein the input signal is a differential quadrature phase shift keying modulated signal.

29. A method according to claim 28, wherein the input signal includes a NICAM 728 signal.

30. A method according to claim 29 for demodulating an I system signal in which the coefficients of the I and Q channel matched fillers are:

HI(0) =	5/256	HQ(0) =	2/256
HI(1) =	-2/256	HQ(1) =	5/256
HI(2) =	-6/256	HQ(2) =	2/256
HI(3) =	0/256	HQ(3) =	-3/256
HI(4) =	1/256	HQ(4) =	1/256
HI(5) =	-9/256	HQ(5) =	0/256
HI(6) =	-2/256	HQ(6) =	-18/256
HI(7) =	32/256	HQ(7) =	-11/256
HI(8) =	28/256	HQ(6) =	40/256
HI(9) =	-46/256	HQ(9) =	52/256
HI(10) =	-80/256	HQ(10) =	-38/256
HI(11) =	20/256	HQ(11) =	-106/256
HI(12) =	123/256	HQ(12 =	-12/256
HI(13) =	49/256	HQ(13) =	127/256
HI(14) =	-113/256	HQ(14) =	86/256
HI(15) =	-113/256	HQ(15) =	-87/256

HI(16) =	49/256	HQ(16) =	-127/256
HI(17) =	123/256	HQ(17) =	12/256
HI(18) =	20/256	HQ(18) =	106/256
HI(19) =	-80/256	HQ(19) =	38/256
HI(20) =	-46/256	HQ(20) =	-52/256
HI(21) =	28/256	HQ(21) =	-40/256
HI(22) =	32/256	HQ(22) =	11/256
HI(23) =	-3/256	HQ(23) =	18/256
HI(24) =	-9/256	HQ(24) =	0/256
HI(25) =	1/256	HQ(25) =	-1/256
HI(26) =	0/256	HQ(26) =	3/256
HI(27) =	-6/256	HQ(27) =	-1/256
HI(28) =	-2/256	HQ(28) =	-4/256
HI(29) =	5/256	HQ(29) =	-2/256

31. A method according to claim 29 for demodulating a B or G system signal in which the coefficients of the I and Q channel matched filters are:

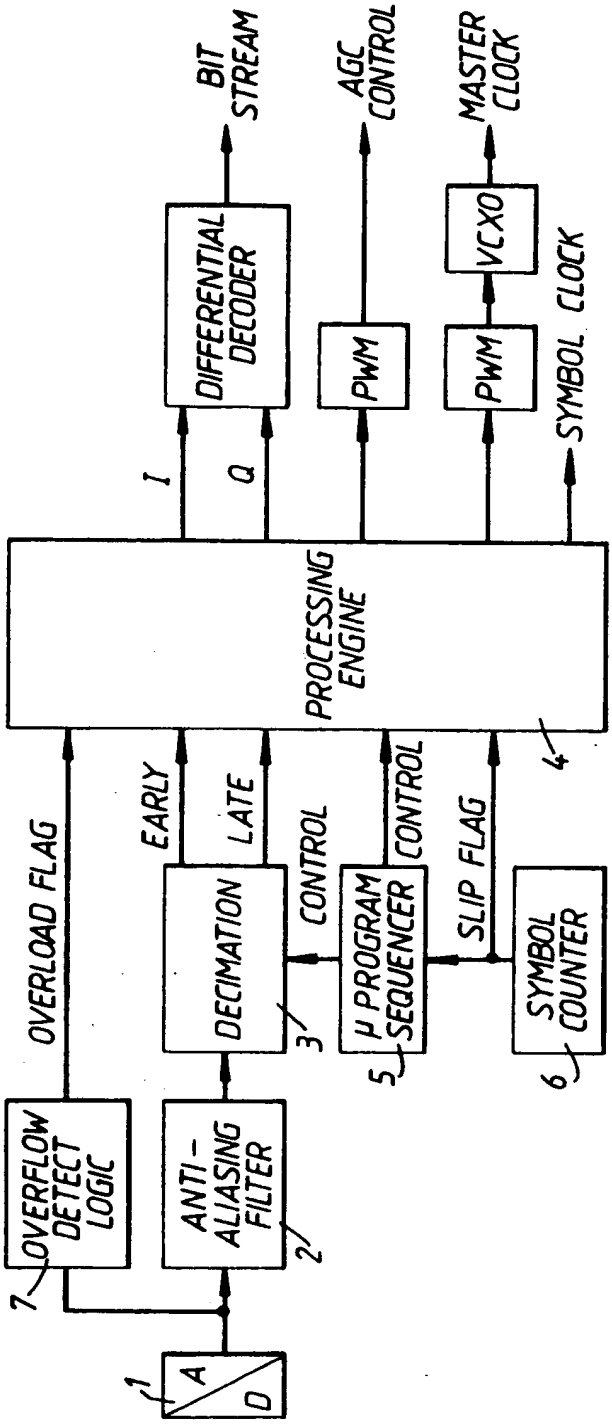
HI(0) =	22/256	HQ(0) =	3/256
HI(1) =	18/256	HQ(1) =	9/256
HI(2) =	8/256	HQ(2) =	18/256
HI(3) =	-3/256	HQ(3) =	29/256
HI(4) =	-16/256	HQ(4) =	37/256
HI(5) =	-30/256	HQ(5) =	38/256
HI(6) =	-44/256	HQ(6) =	27/256
HI(7) =	-56/256	HQ(7) =	5/256
HI(8) =	-62/256	HQ(8) =	-25/256
HI(9) =	-57/256	HQ(9) =	-55/256
HI(10) =	-36/256	HQ(10) =	-77/256
HI(11) =	-2/256	HQ(11) =	-86/256
HI(12) =	39/256	HQ(12) =	-79/256
HI(13) =	75/256	HQ(13) =	-55/256
HI(14) =	97/256	HQ(14) =	-20/256
HI(15) =	97/256	HQ(15) =	20/256
HI(16) =	75/256	HQ(16) =	55/256
HI(17) =	39/256	HQ(16) =	79/256

HI(18) =	-3/256	HQ(18) =	86/256
HI(19) =	-36/256	HQ(19) =	77/256
HI(20) =	-56/256	HQ(20) =	54/256
HI(21) =	-62/256	HQ(21) =	24/256
HI(22) =	-56/256	HQ(22) =	-5/256
HI(23) =	-44/256	HQ(23) =	-27/256
HI(24) =	-30/256	HQ(24) =	-38/256
HI(25) =	-16/256	HQ(25) =	-37/256
HI(26) =	-3/256	HQ(26) =	-29/256
HI(27) =	9/256	HQ(27) =	-18/256
HI(28) =	18/256	HQ(28) =	-9/256
HI(29) =	22/256	HQ(29) =	-3/256

and the outputs of the matched filters are subjected to feedforward equalization respectively for the I and Q channels having the coefficients:

FFEI(O) = -52/256 FFEQ(0) = -52/256
FFEI(1) = 1 FFEQ(1) = 1
FFEI(2) = -52/256 FFEQ(2) = -52/256

32. A method of processing a signal substantially as described herein and as illustrated by the accompanying drawings.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D
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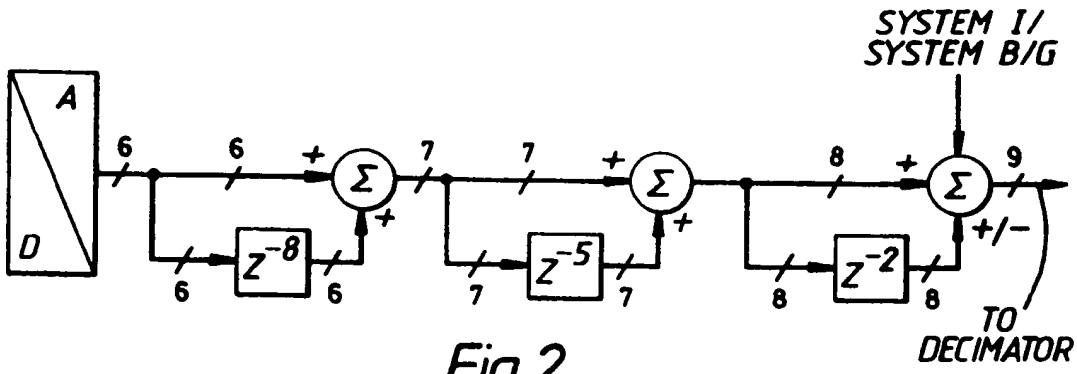
7
ANTI-ALIASING FILTER
2
DECIMATION
3
EARLY
LATE
CONTROL
μ PROGRAM SEQUENCER
5
CONTROL
SLIP FLAG
SYMBOL COUNTER
6
OVERLOAD FLAG
PROCESSING ENGINE
4
I
Q
DIFFERENTIAL DECODER
PWM
PWM
VCXO
BIT STREAM
AGC CONTROL
MASTER CLOCK
SYMBOL CLOCK

Fig.1.


SYSTEM I/
SYSTEM B/G
A
D
6
6
+
Σ
7
7
+
Σ
8
+
Σ
9
+/-
+
+
+
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Z^{-5}
Z^{-2}
6
6
7
7
8
8
TO
DECIMATOR

Fig.2.

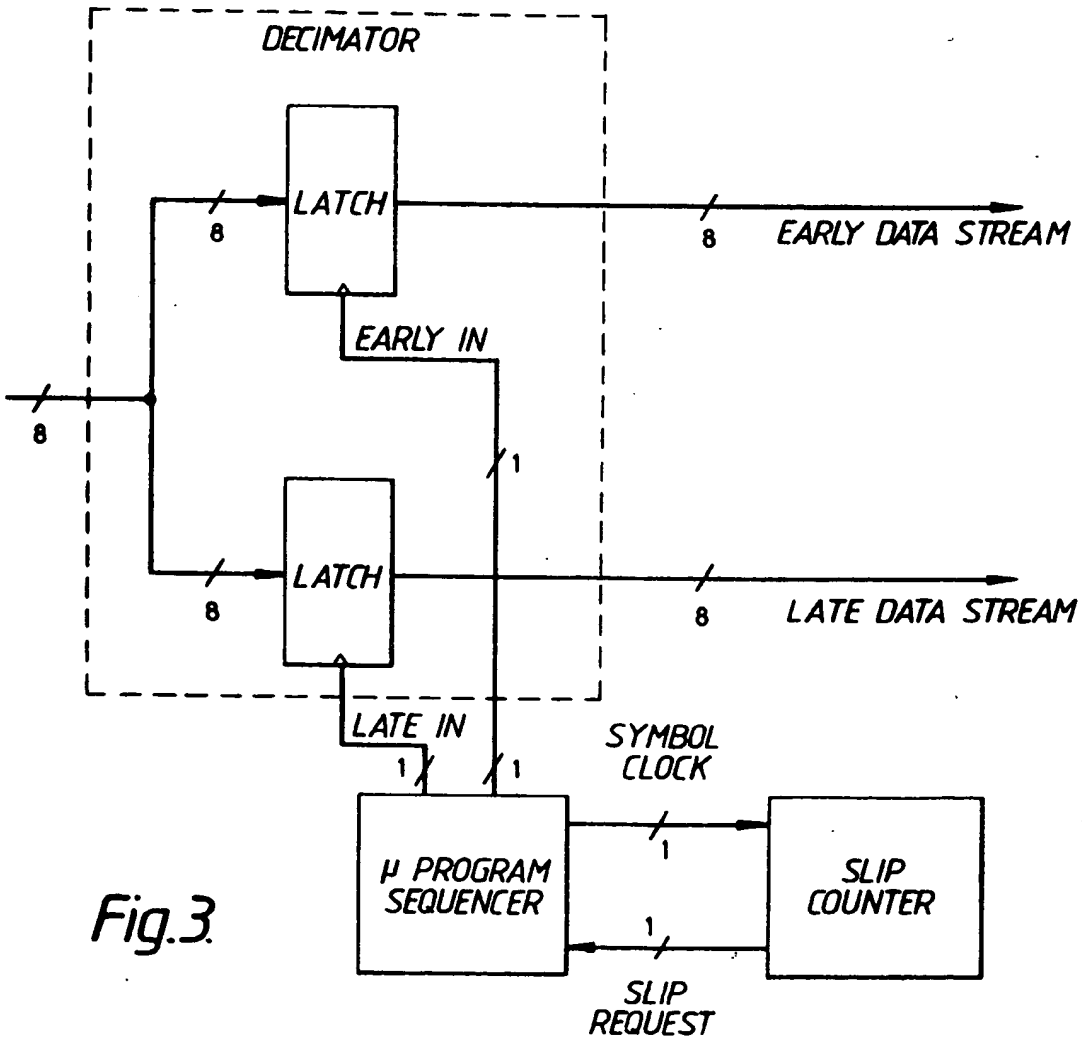
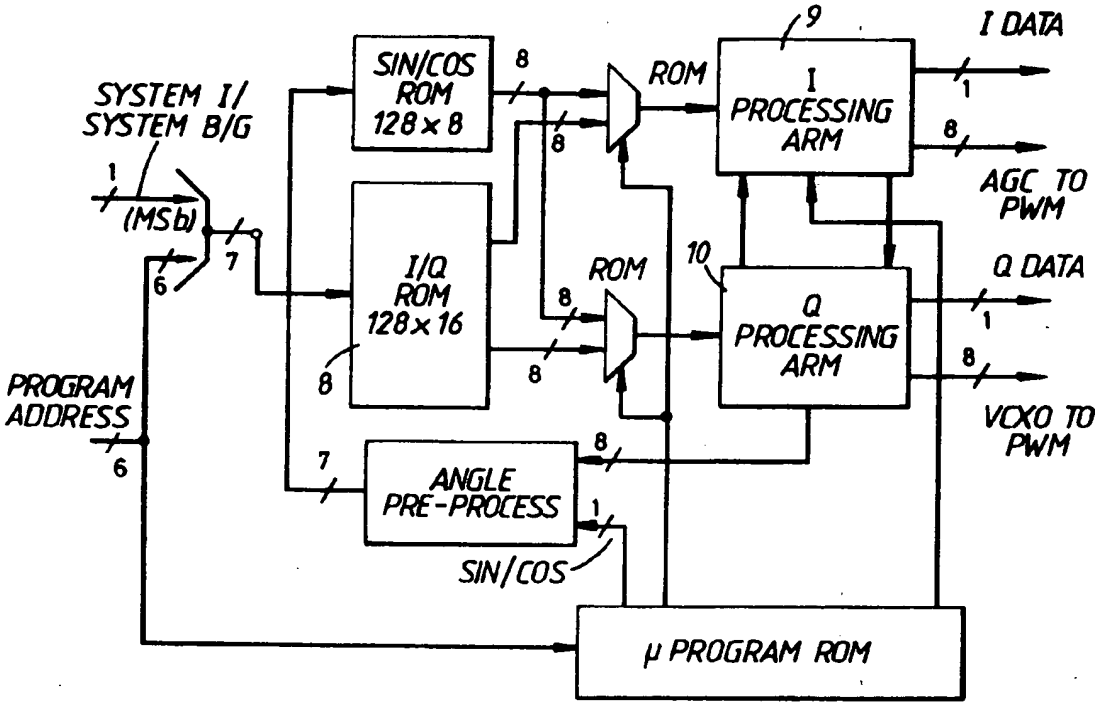

DECIMATOR
LATCH
8
8
EARLY DATA STREAM
EARLY IN
8
1
LATCH
8
8
LATE DATA STREAM
LATE IN
SYMBOL
CLOCK
1
1
μ PROGRAM
SEQUENCER
1
SLIP
COUNTER
1
SLIP
REQUEST

Fig.3.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SYSTEM B/G
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(MSb)
6
7
PROGRAM
ADDRESS
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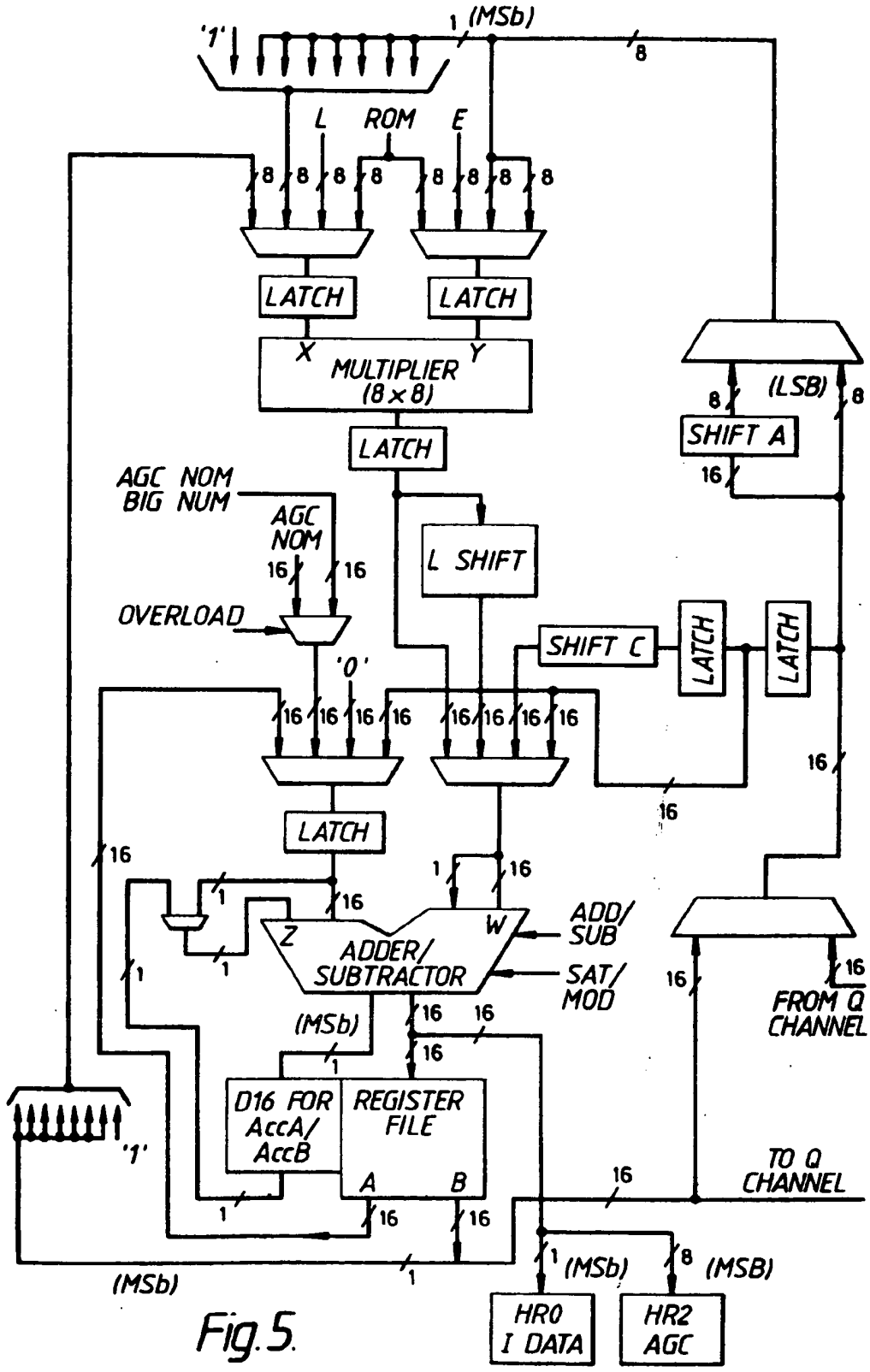
SIN/COS
ROM
128 x 8
8
I/Q
ROM
128 x 16
8
8
ROM
8
8
ROM
9
I
PROCESSING
ARM
10
Q
PROCESSING
ARM
I DATA
1
8
AGC TO
PWM
Q DATA
1
8
VCXO TO
PWM
7
ANGLE
PRE-PROCESS
8
1
SIN/COS
μ PROGRAM ROM

Fig.4.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8
L ROM E
8 8 8 8 8 8 8 8
LATCH
LATCH
X
Y
MULTIPLIER (8 x 8)
LATCH
8
(LSB)
8
SHIFT A
16
AGC NOM BIG NUM
AGC NOM
16
16
L SHIFT
OVERLOAD
'0'
SHIFT C
LATCH
LATCH
16 16 16 16 16 16 16 16
16
16
LATCH
16
1
16
1
16
1
1
Z
W
ADD/ SUB
ADDER/ SUBTRACTOR
SAT/ MOD
16
16
FROM Q CHANNEL
(MSb)
1
16 16
16
D16 FOR AccA/ AccB
REGISTER FILE
A
B
'1'
TO Q CHANNEL
16
1
16
16
(MSb)
1
(MSb)
1
8
(MSb)
HR0 I DATA
HR2 AGC

Fig. 5.

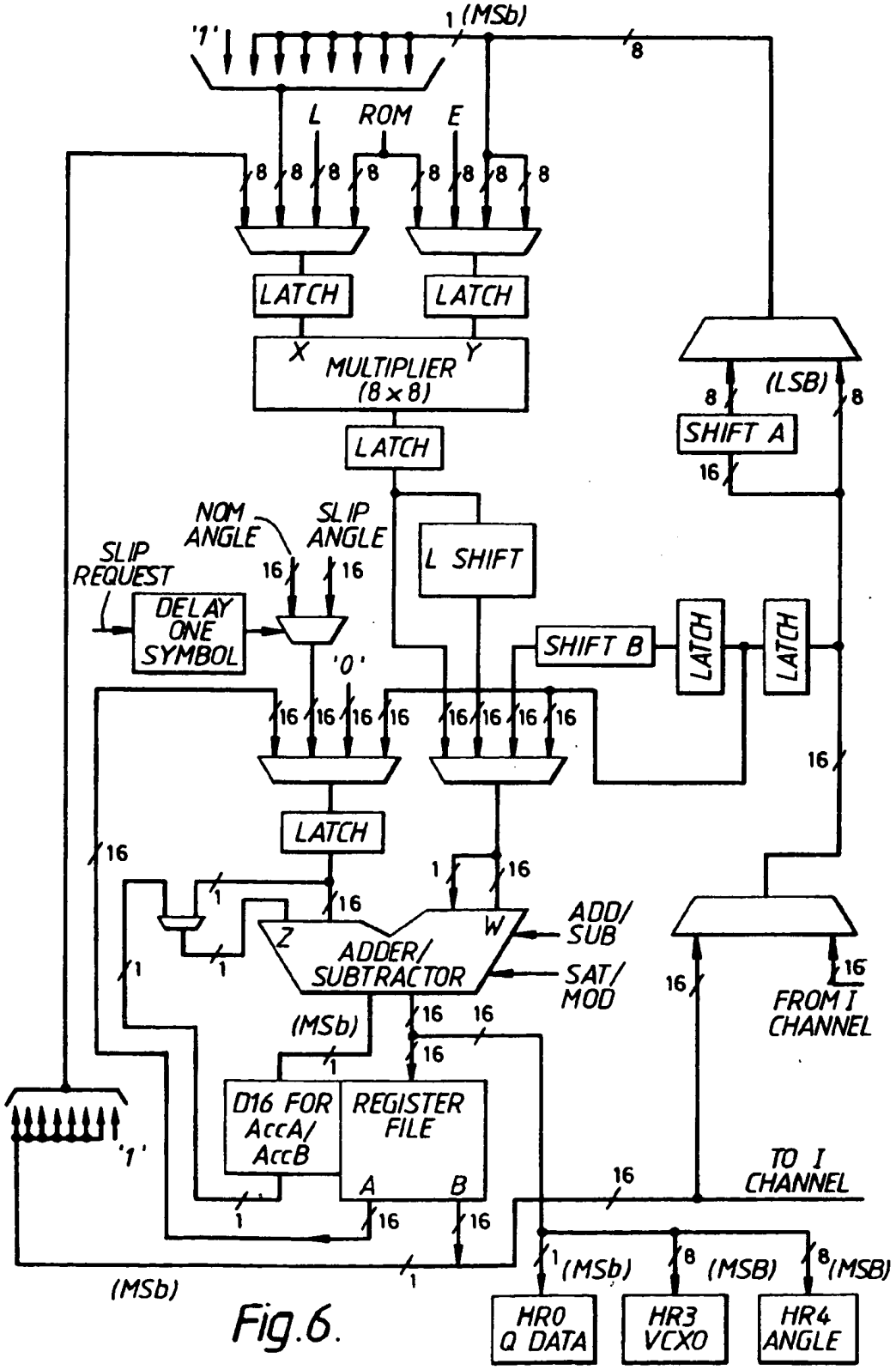
'1'
1 (MSb)
8
L ROM E
LATCH
LATCH
X
MULTIPLIER (8 x 8)
Y
LATCH
8
(LSB)
8
SHIFT A
16
NOM ANGLE
SLIP ANGLE
SLIP REQUEST
DELAY ONE SYMBOL
L SHIFT
SHIFT B
LATCH
LATCH
'0'
LATCH
ADD/ SUB
SAT/ MOD
Z
W
ADDER/ SUBTRACTOR
(MSb)
FROM I CHANNEL
D16 FOR AccA/ AccB
REGISTER FILE
A
B
'1'
TO I CHANNEL
(MSb)
(MSb)
(MSB)
(MSB)
HR0 Q DATA
HR3 VCXO
HR4 ANGLE

Fig.6.

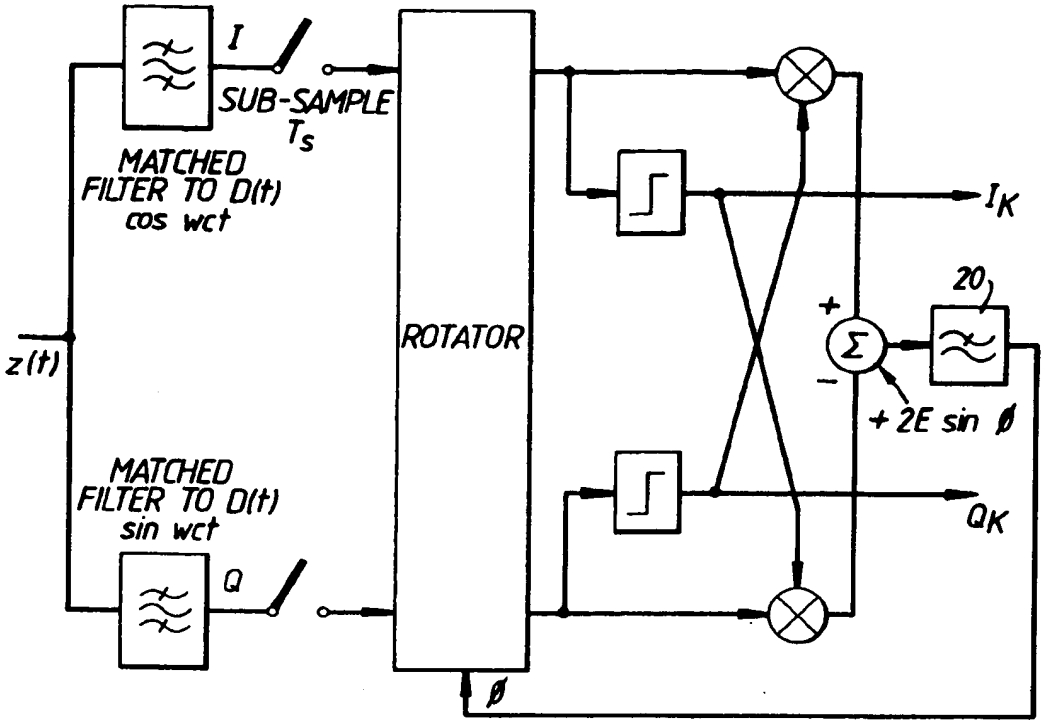

Fig.7

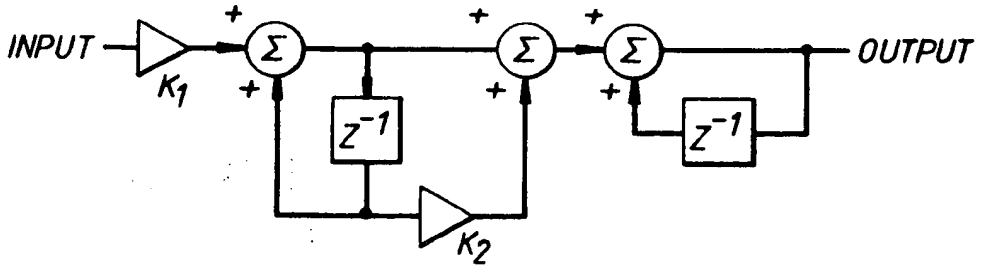

Fig.8

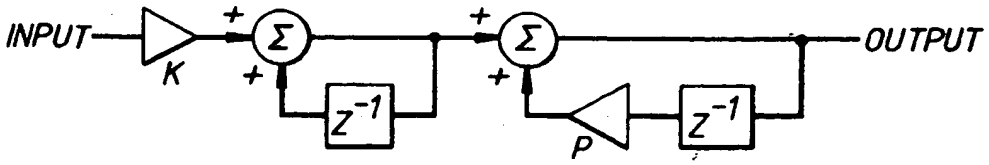

Fig.9

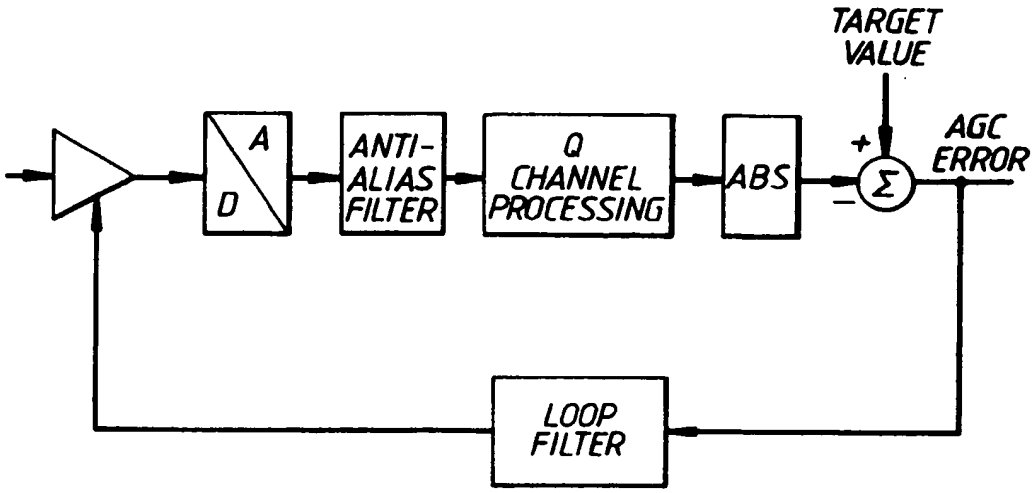
TARGET VALUE
A
D
ANTI-ALIAS FILTER
Q CHANNEL PROCESSING
ABS
+
−
Σ
AGC ERROR
LOOP FILTER

Fig.10.

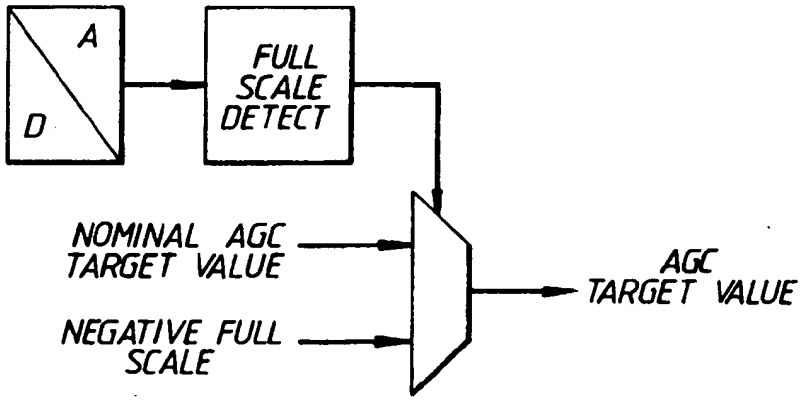
A
D
FULL SCALE DETECT
NOMINAL AGC TARGET VALUE
NEGATIVE FULL SCALE
AGC TARGET VALUE

Fig.11.

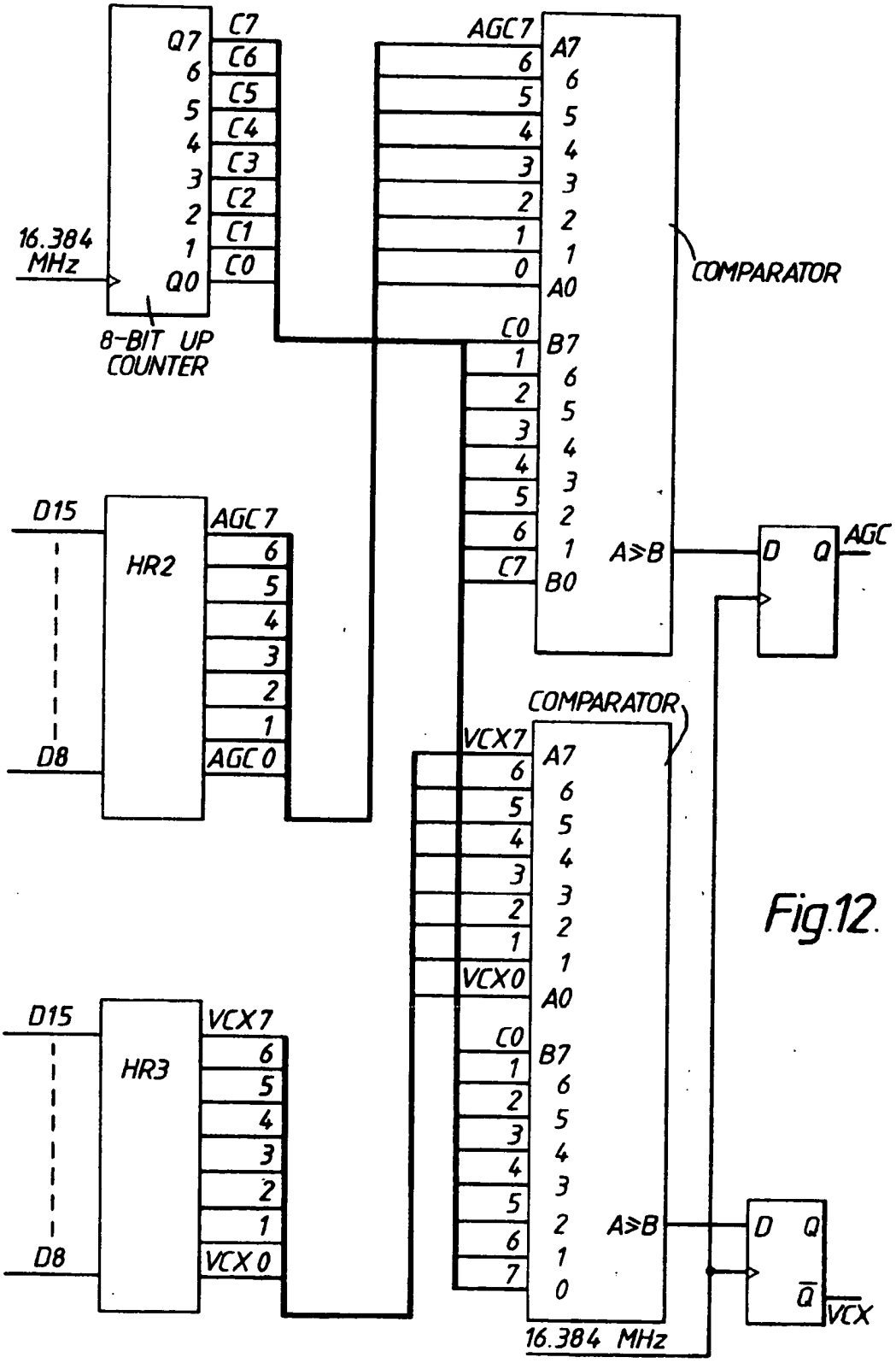
16.384 MHz
Q7
6
5
4
3
2
1
Q0
C7
C6
C5
C4
C3
C2
C1
C0
8-BIT UP COUNTER
AGC7
6
5
4
3
2
1
0
C0
1
2
3
4
5
6
C7
A7
6
5
4
3
2
1
A0
B7
6
5
4
3
2
1
B0
A≥B
COMPARATOR
D
Q
AGC
D15
D8
HR2
AGC7
6
5
4
3
2
1
AGC0
VCX7
6
5
4
3
2
1
VCX0
C0
1
2
3
4
5
6
7
COMPARATOR
A7
6
5
4
3
2
1
A0
B7
6
5
4
3
2
1
0
A≥B
16.384 MHz
D15
D8
HR3
VCX7
6
5
4
3
2
1
VCX0
D
Q
Q̄
VCX

Fig.12.

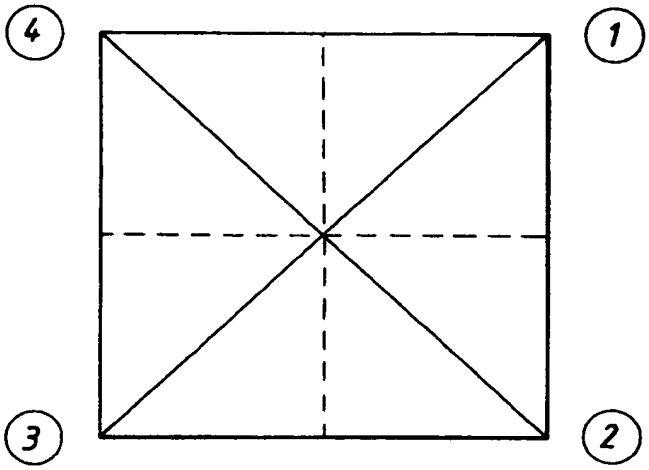
4
1
3
2

Fig.13.

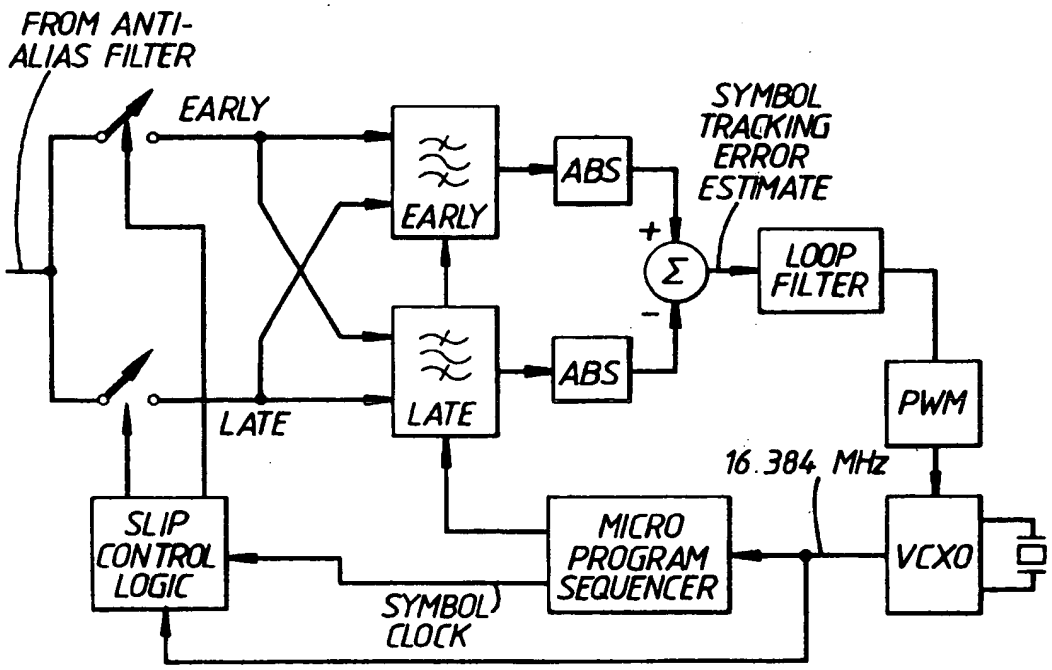
FROM ANTI-ALIAS FILTER
EARLY
LATE
EARLY
LATE
ABS
ABS
+
Σ
−
SYMBOL TRACKING ERROR ESTIMATE
LOOP FILTER
PWM
16.384 MHz
VCXO
MICRO PROGRAM SEQUENCER
SLIP CONTROL LOGIC
SYMBOL CLOCK

Fig.15.

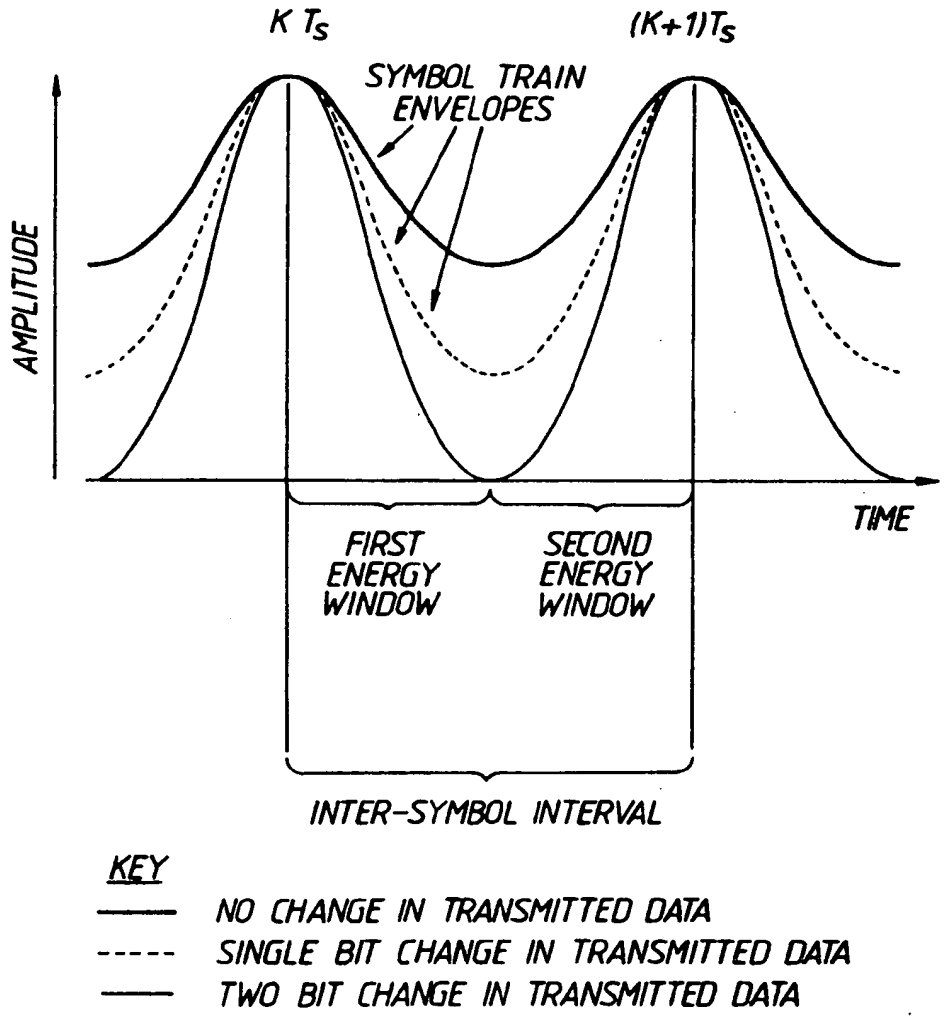
K T_S
(K+1)T_S
SYMBOL TRAIN ENVELOPES
AMPLITUDE
TIME
FIRST ENERGY WINDOW
SECOND ENERGY WINDOW
INTER-SYMBOL INTERVAL
KEY
NO CHANGE IN TRANSMITTED DATA
SINGLE BIT CHANGE IN TRANSMITTED DATA
TWO BIT CHANGE IN TRANSMITTED DATA

Fig.14.

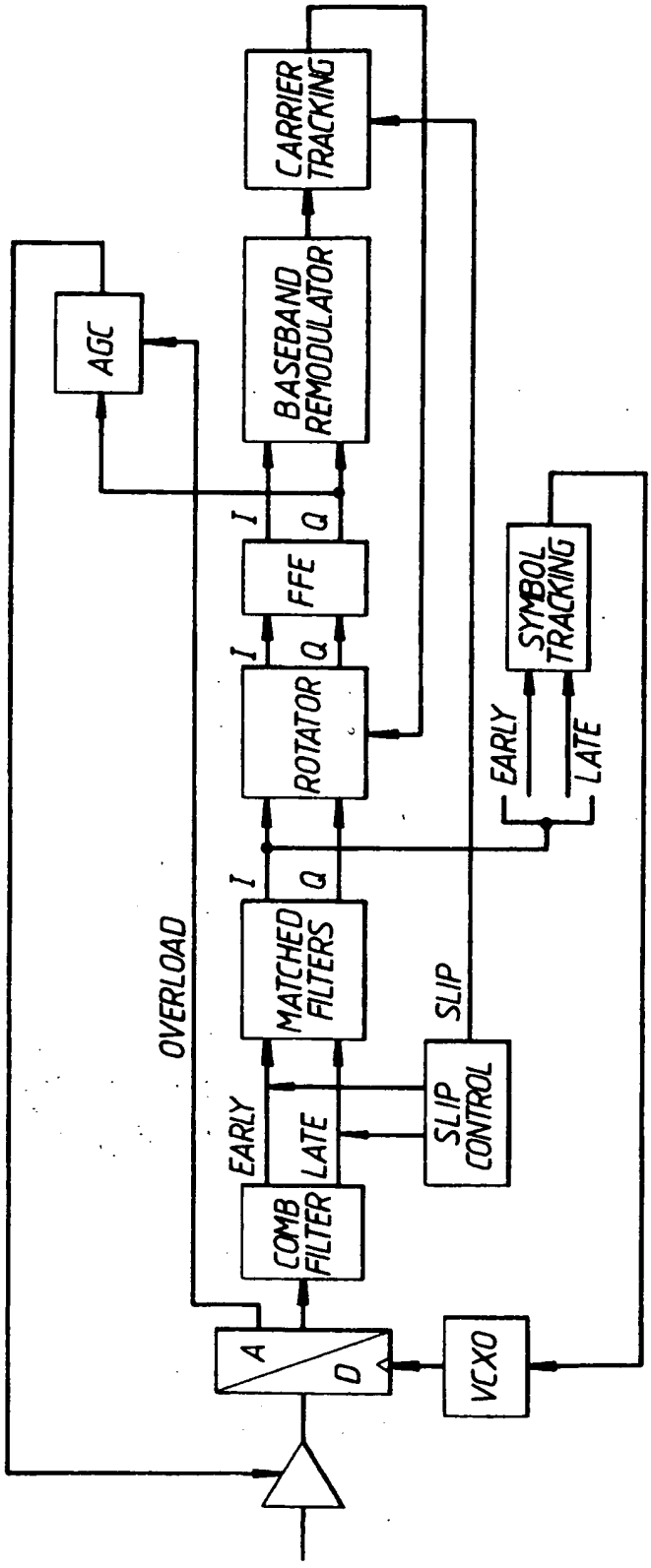
CARRIER TRACKING
BASEBAND REMODULATOR
AGC
I
Q
FFE
I
Q
ROTATOR
I
Q
MATCHED FILTERS
SYMBOL TRACKING
EARLY
LATE
OVERLOAD
SLIP
SLIP CONTROL
EARLY
LATE
COMB FILTER
A
D
VCXO

Fig.16.

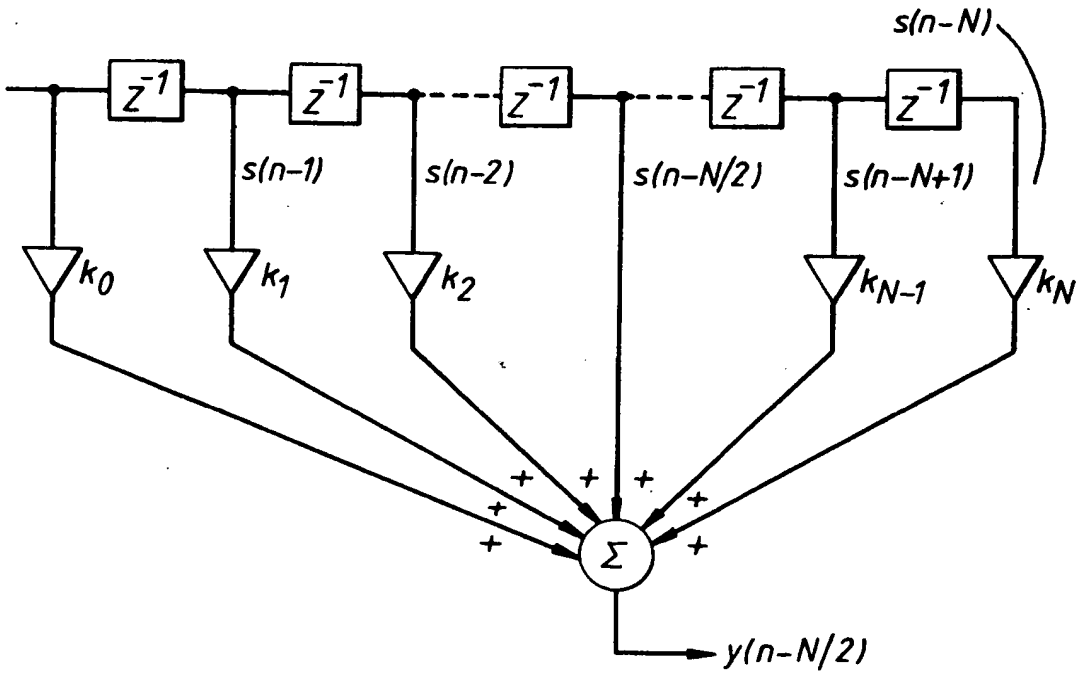

Fig.17.